WHAT IS CLAIMED IS:

1. A static random access memory (SRAM) device comprising:

a first transistor pair coupled between a supply voltage line and GROUND;

a second transistor pair coupled between the supply voltage line and GROUND;

a first access transistor coupled to a word line, a first bitline and a common node of the second transistor pair;

a second access transistor coupled to the word line, a second bitline and a common node of the first transistor pair; and

a bias transistor coupled to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair.

2. The SRAM device of claim 1, wherein the bias transistor comprises an NMOS transistor having a source coupled to GROUND.

3. The SRAM device of claim 2, wherein a drain of the bias transistor is coupled to the body of the one transistor of the first transistor pair and to the body of the one transistor of the second transistor pair.

4. The SRAM device of claim 1, wherein the bias transistor applies a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on a mode of the memory device.

5. The SRAM device of claim 4, wherein the supply voltage line receives a different supply voltage based on the mode of the memory device.

6. The SRAM device of claim 1, wherein a gate of the bias transistor is coupled to a signal line to receive a STANDBY signal indicative of a STANDBY state of the memory device.

7. The SRAM device of claim 1, wherein the bias transistor turns ON based on a STANDBY signal applied to a gate of the bias transistor.

8. The SRAM device of claim 1, wherein the one transistor of the first transistor pair comprises a PMOS transistor and the one transistor of the second transistor pair comprises another PMOS transistor.

9. A static random access memory (SRAM) device comprising:

a first SRAM memory cell having a cross-coupled inverter configuration, the cross-coupled inverter configuration including at least four transistors;

a supply voltage line to provide a supply voltage to two transistors of the first SRAM memory cell; and

a switching device to apply a forward body bias to the two transistors of the cross-coupled inverter configuration of the first SRAM memory cell.

10. The SRAM device of claim 9, further comprising a power control unit to change the supply voltage on the supply voltage line based on a mode of the first SRAM memory cell.

11. The SRAM device of claim 10, wherein the power control unit further to control switching of the switching device based on the mode of the first SRAM memory cell.

12. The SRAM device of claim 10, wherein the switching device comprises an NMOS transistor having a source coupled to GROUND and a gate coupled to the power control unit.

13. The SRAM array device of claim 12, wherein a drain of the NMOS transistor is coupled to a body of each of the two transistors.

14. The SRAM array device of claim 12, wherein a gate of the NMOS transistor receives a STANDBY signal from the power control unit indicative of a STANDBY state of the first SRAM memory cell.

15. The SRAM array device of claim 12, wherein the NMOS transistor turns ON based on a STANDBY signal applied to the gate of the NMOS transistor.

16. The SRAM device of claim 9, further comprising a second SRAM memory cell having a cross-coupled inverter configuration, the cross-coupled inverter configuration of the second SRAM memory cell including at least four transistors, the supply voltage line to provide supply voltage to two transistors of the second SRAM memory cell.

17. The SRAM device of claim 16, wherein the switching device to apply a forward body bias to the two transistors of the cross-coupled configuration of the second SRAM memory cell.

18. An electronic system comprising:

a processor device to process data; and

a static random access memory (SRAM) device to store the data;

a power control unit to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device, the SRAM device including:

a switching device to apply a forward bias to transistors within the SRAM device based on the signal provided by the power control unit indicative of the mode.

19. The electronic system of claim 18, wherein the switching device applies the forward body bias by coupling a body of each of the transistors to GROUND.

20. The electronic system of claim 18, wherein applying the forward bias to the transistors increases a static noise margin.